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PARTIALLY DEPLETED SOI MOSFET DEVICE

Abstract

A partially depleted SOI MOS deviceincludes a well of first conductivity type isolated in a thin film body of an SOI substrate. The SOI substrate encompasses the thin film body, a support substrate, and a buried oxide layer interposed between the thin film body and the support substrate. Agate dielectric layer is disposed on a surface of the well.A polysilicon gate is patterned on thegate dielectric layer. The polysilicon gate consists of a first gate section of first conductivity type overlapping with an extended well region of the well and a second gate section of second conductivity type lying across the well, whereby a tunneling connection is formed between the first gate section and theextended well region of said well. Source and drain regions of second conductivity typeare formedon opposite sides of thesecond gate section.